XJTAG DFT Assistant

Free ‘Design For Test’ (DFT) plugin to reduce board re-spins

The new XJTAG® DFT Assistant software plugin allows design engineers to identify and correct potential JTAG testability problems early in the design cycle. Because many IC packages are inaccessible for testing using physical probes, failure to provide JTAG test access to these chips could result in a board re-spin and an expensive project delay.

XJTAG DFT Assistant helps you validate the correct implementation of boundary scan chains, as well as provides compliance to ‘Design For Test’ best practices. What’s more, JTAG compliance can also unlock a range of other benefits for your board, which include faster prototype debug and device programming, as well as faster and more cost-effective manufacturing testing.

Key Benefits

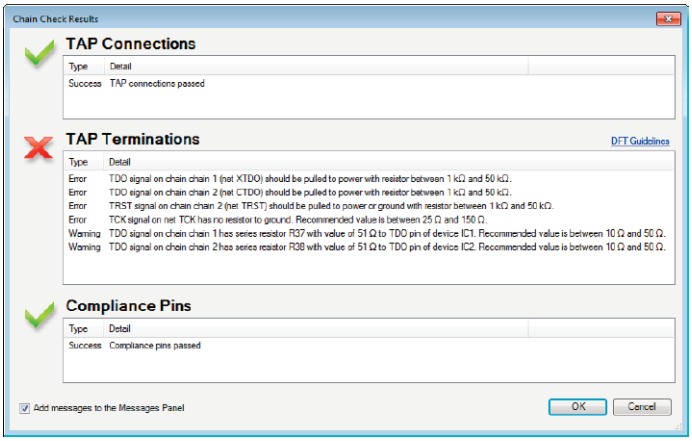
- Carry out a DFT analysis for Boundary Scan access from within the schematic capture environment
- Avoid errors early in the development cycle, reducing PCB re-spins or modifications
- Understand where your JTAG chain provides test access through color-coded views
- Extend your Boundary Scan test coverage by correctly implementing JTAG chains
- Improve the production process and reduce your time-to-market
- Export all data to XJDeveloper for further test development (full or evaluation license for XJTAG tools required)

XJTAG Chain Checker

After a quick 4-step board setup, the XJTAG Chain Checker feature analyses the netlist and finds a routable scan chain. It also offers a unique DFT feature: checking that the TAP signals are correctly terminated.

XJTAG Chain Checker identifies potential errors and warnings found on JTAG chains, including:

- **Connection errors** if any of the JTAG Test Access Point (TAP) signals are connected to the wrong pin(s) on a JTAG-compliant IC.
- **Termination warnings** if any of the TAP signals are not terminated as recommended.
- **Compliance pin errors** if they are incorrectly pulled high or low, or are left floating.

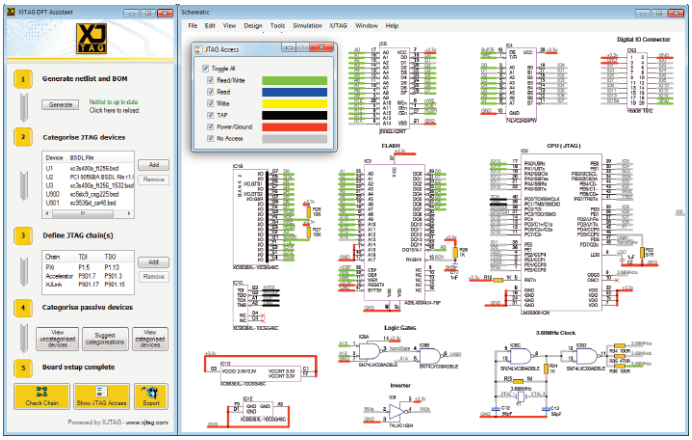


The XJTAG Chain Checker identifies and categorizes faults and warnings in the boundary scan chain(s)

XJTAG Access Viewer

The XJTAG DFT Assistant extension also identifies the extent of JTAG access across an entire schematic. This is overlaid directly onto the schematic using the XJTAG Access Viewer feature, allowing you to understand your test coverage at an early stage in the design. You can highlight the nets individually on the schematic by JTAG access, to show: read, write, power/ground and no access.

By visualising the extent of JTAG access, you can easily see which components are accessible using boundary scan and where changes need to be made to extend test coverage further.



The XJTAG Access Viewer provides a clear indication of test access at any point during the design process