



## PRESS RELEASE

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### New: RISC-V – high-calibre panel discussion

- **Benefits and drawbacks of using open architectures**
- **Outstanding international speakers**

**For the first time at embedded world, there will be a high-calibre panel discussion about the instruction set architecture RISC-V. RISC-V is an open-source instruction set architecture that can be used free of charge thanks to the BSD licence. The project began back in 2010 at the University of California, Berkeley, and is already being co-developed and promoted by hardware and software developers worldwide, including leading semi-conductor manufacturers. In addition, a large community has formed for the development of the ecosystem around the CPU architecture. The panel discussion forum in Hall 3A on 27 February 2019 will not only look at the latest state of the art but will also explore the benefits and drawbacks of these kinds of open architectures.**

Four established international experts will debate the topic of RISC-V in a discussion moderated by Frank Riemenschneider, editor-in-chief of the specialist journal Design & Elektronik. They are Cesare Garlati, Chief Security Strategist, prpl Foundation, Markus Levy, Head of AI and Machine Learning Technologies, NXP Semiconductors, Ted Marena, Director, RISC-V Ecosystem, Western Digital and Tim Whitfield, VP Strategy, Embedded and Automotive, ARM.

Professor Axel Sikora, chair of the advisory committee of embedded world and the embedded world conference, is looking forward to the panel discussion: “RISC-V is a hot topic, because comparable to the battle between Linux and Microsoft, an attempt is being made to challenge the market position of ARM. The discussion at the forum with top-class international players is sure to be very interesting. For those who want to delve a little deeper into the technology, the conference will also devote one and half days to presentations and classes exclusively on RISC-V.”

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**Brief details of the experts****Cesare Garlati, Chief Security Strategist, prpl Foundation**

Cesare Garlati is an internationally renowned expert in information security. Former Vice President of mobile security at Trend Micro, Cesare currently serves as Chief Security Strategist at prpl Foundation – a technology non-profit dedicated to enabling security and interoperability of embedded systems. Cesare is a long-time supporter of the RISC-V Foundation, a key member of the RISC-V security group and co-founder of Hex Five Security – the creator of the first trusted execution environment for RISC-V. Cesare holds a U.C. Berkeley MBA, a Master in Electrical Engineering and Computer Sciences, professional certifications from Microsoft, Cisco and Oracle, and is a Fellow of the Cloud Security Alliance, where he founded and chaired the Mobile Security and IoT Security groups.

**Markus Levy, Head of AI and Machine Learning Technologies, NXP Semiconductors**

Markus Levy joined NXP in 2017 as the Director of AI and Machine Learning Technologies. In this position, he is primarily focused on the strategy, development, and marketing of AI and machine learning capabilities for NXP's microcontroller and i.MX product lines. At NXP, Markus is also responsible for driving the RISC-V ecosystem. Previously, Markus was chairman of the board of EEMBC, which he founded and ran as the President since April 1997. Mr. Levy was also president of the Multicore Association, which he co-founded in 2005. He was previously a Senior Analyst at Microprocessor Report and an editor at EDN magazine. Markus began his career at Intel Corporation, as both a Senior Applications Engineer and customer training specialist for Intel's microprocessor and flash memory products.

**Ted Marena, Director, RISC-V Ecosystem, Western Digital**

Ted Marena is responsible for evangelizing RISC-V and accelerating the build out of the RISC-V ecosystem. He has over 25 years' experience in electronics and excels at business development, marketing and revenue growth. Marena previously worked at Microsemi where he was awarded the Rock Star status for marketing the SoC FPGA product lines. He was elected Marketing Chair for the RISC-V organisation in 2016. Marena was awarded US patent 9009379 in 2015. He earned Innovator of the Year in 2014 when he worked for Lattice Semiconductor. Marena has defined, created and executed unique marketing solutions for data centre, consumer, machine learning, industrial IoT and automotive applications. Marena started working as a design engineer, field application engineer and a sales manager before



he moved to marketing and business development. His understanding of the complete electronics design cycle has earned him a reputation as an expert marketer in the electronics industry. Marena holds a Bachelor of Science in electrical engineering Magna Cum Laude from the University of Connecticut and a MBA from Bentley University's Elkin B. McCallum Graduate School of Business.

### **Tim Whitfield, VP Strategy, Embedded and Automotive, ARM**

Tim Whitfield is vice president strategy, Embedded and Automotive Line of Business at ARM, where he leads a team looking at business and technology strategy for the ARM IP group. He has worked at ARM for more than 15 years, initially leading hardware engineering teams building IP and silicon implementations. More recently he spent five years in Taiwan establishing an engineering design centre and working with local ecosystem partners on advanced process technology. Before working at ARM, Tim worked at Fujitsu Telecommunications and GEC in the UK.

### **Free entry to embedded world 2019**

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